REMARKS

In an Office Action mailed April 20, 2004, pending claims 1, 2, 4, 5, 7-25 and 34 were rejected and the rejection was made final. In response, Applicants are herein amending claims 1, 9, 15, 17 and 34, canceled claims 13 and 22, added claims 35 and 36, and respectfully request the reconsideration and allowance of claims 1, 2, 4, 5, 7-12, 14-21, 23-25 and 34-36.

Applicants have not received a confirmation from the Examiner of consideration of an Information Disclosure Statement (IDS) submitted mailed by Certificate of Mailing on July 11, 2003. The IDS contained references BA through BG. Applicants request confirmation of consideration of these references in the next Office Action response.

Claims 1, 4, 5 and 7-16 were rejected under 35 U.S.C. 112, first paragraph. Claim 1 was rejected in connection with the recital "removing a portion of the conductive layer and the second semiconductor layer to physically separate a first gate region and a second gate region". While acknowledging that the specification teaches two different removing steps, the claim is rejected for not teaching one removing step that removes both recited layers. However, claim 1 is not expressly reciting removing a portion of the conductive layer and the second semiconductor layer with a single step. Rather claim 1 is reciting the removal of both layers. The specification teaches and fully discloses an embodiment for implementing this function. Additional undisclosed embodiments, within the ordinary skill in the art, may be used, such as the simultaneous removal of these layers. However, 35 U.S.C. 112, first paragraph, does not require the disclosure of all embodiments to perform a recited function. The limitation of "simultaneously" removing these layers is improperly being read into the claim recital. Because claim 1 is fully supported in an enabling manner by the specification, Applicants request the withdrawal of the stated rejection of claim 1.

Dependent claim 10 was rejected for lack of support in the specification for "electrically

coupling the first gate region and the second gate region". As an example, the specification at page 11, lines 5 and 6 teach that a metal layer 66 electrically connects the first gate 46 with the second gate 48. Illustrated in FIG. 14 is the metal layer 66 and gates 46 and 48 are illustrated by arrows pointing to the gate regions. This electrical coupling is an optional feature. FIG. 15 illustrates that the electrical coupling has been removed and page 11, line12 states that the processing to disconnect the coupling is optional. Dependent claim 10 is fully supported by the specification and Applicants request the withdrawal of the rejection.

Claim 15 was rejected for having inadequate antecedent basis for the term "electrode region". In response, Applicants have amended claim 15 to recite "gate" rather than "electrode". Withdrawal of the rejection is requested.

Claims 9 and 13 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Dependent claim 9 was rejected for not correlating the recited first and second directional implants of claim 1 with the recited "after doping the second semiconductor layer". Claim 9 is herein amended to recite "after performing the second directional implant". Withdrawal of the rejection of claim 9 is therefore requested.

Dependent claim 13 was rejected for containing a repetitive limitation to a recitation in claim 1. In response, Applicants have herein canceled claim 13, thereby removing the basis for the rejection.

Claims 1, 2, 4, 5, 7-14, 16-25 and 34 were rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (U.S. Patent 6,472,258) in view of Fried et al. (U.S. Pub 2003/0113970). The Adkisson et al. reference is relied upon for its teaching of a dual gate trench transistor and admittedly does not teach implanting a layer with two implant species (Page 4, paragraph 7 of the Office Response mailed April 20, 2004). Fried et al. is cited for the

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proposition of a transistor process having a continuous gate material implanted by implants 20 and 22. The rejection is based on the combination of these two references wherein the directional implant of Fried et al. is used on the structure of Adkisson et al.

In the Office Action mailed April 20, 2004, Applicants were stated to not have argued why there is no incentive to combine Adkisson et al. with Fried et al. Applicants will now correct that omission. Adkisson et al. do not teach the doping of the gate polysilicon and only teach at Col. 3, lines 6-10 the doping of the channel in a manner to be fully depleted. The silence in Adkisson et al. on doping of the gate polysilicon does not suggest combining the use of an angled implant, either from the Fried et al. reference or any other reference where angled implants are used. Additionally, even if the gate polysilicon of Adkisson et al. is angle implanted, due to the horizontal surfaces of the gate polysilicon adjacent the silicon channel the gate will be counterdoped and subject to the noted prior art performance issues.

It should also be noted that the transistor of Fried et al. is exemplary of the prior art characterization at Applicants' specification at page 2, lines 18-25, wherein a transistor is formed that has cross migration of dopants in the gate. For example, in FIG. 3B of Fried et al. the horizontal portions of layer 28 contain cross doping concentrations which leads to a transistor having a high resistivity gate. It should also be noted that the transistor structures of Adkisson et al., whether FIG. 2, FIG. 3 or FIG. 4, each have horizontal surfaces adjacent the vertical silicon channel. Therefore, while there is absolutely no suggestion by Adkisson et al. to dope the gate, if a directional implant is performed on any of the Adkisson et al. structures, the exposed horizontal surface of the left and right gate polysilicon material will be counterdoped and have the associated transistor performance issues mentioned above in connection with the Fried et al. structure. Note that the FIG. 3 embodiment of the Adkisson et al. structure uses a metal outer spacer positioned away from the channel. Because these spacers are metal, metal cannot be doped. Further, any injection of external material into a metal will not have similar effect as doping a semiconductor, such as modifying conductivity types between N and P types.

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In contrast, in Applicants' recited method a structure is formed wherein the gate material immediately adjacent the channel does not have a horizontal surface. A non-horizontal gate surface is immediately adjacent the channel. As a result, the structure produced by the recited method of claims 1, 2, 4, 5, 7-14, 16-25 and 34 is not counterdoped by the recited angular doping. The recited method provides a structure which has improved threshold voltage control and control of the electrical properties is enhanced.

Even assuming that the angular implanting of Fried et al. is applied to the structure of Adkisson et al, this combination does not teach or suggest the method of claim 1 and does not result in an analogous structure. For example, the step of "providing a second semiconductor layer over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure and having a non-horizontal surface adjoining the semiconductor structure" is not taught by the combination of references. In the rejection of claim 1, the recited "second semiconductor layer" was stated to be layer 20 of Adkisson et al. (page 4, paragraph 7 of the April 20, 2004 Office response). In none of the structures of Adkisson et al. is layer 20 "over and adjacent" the semiconductor structure "and having a non-horizontal surface" as layer 20 only has a horizontal surface. The combination of references does not teach a "second semiconductor layer having a non-horizontal surface adjoining the semiconductor structure". Angled doping is primarily effective when non-horizontal surfaces are doped because the non-horizontal profile adjacent the semiconductor structure substantially prevents the doping of a non-horizontal surface on an opposite side of the semiconductor structure. In addition, in the claimed methods, cross doping of diffusion material is prevented by eliminating at least one horizontal surface where cross doping occurs.

With respect to claim 17, the combination of Adkisson et al. and Fried et al. do not teach or suggest forming the recited second semiconductor layer over and adjacent the semiconductor structure and having the recited three portions wherein the recited second portion is removed after a doping of the first and third portions. While the gate polysilicon region 20 of the Adkisson et al. structure initially overlies the silicon nitride insulating areas prior to being etched

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as shown in the Figures, there is no teaching or suggestion by Adkisson et al. to dope the structure prior to such etching, much less to use angular implants. There is also no teaching by Adkisson et al. of a method to form a semiconductor layer having portions with non-horizontal surfaces. Applicants respectfully request the withdrawal of the rejection of claims 17-21 and 23-25.

Claim 34 was rejected on the same basis stated for claims 1 and 17. Claim 34 is herein amended to recite formation of a semiconductor layer having a first portion and a second portion with respective non-horizontal surfaces adjacent sidewalls of a semiconductor structure. Neither Adkisson et al. nor Fried et al. teach or suggest the recited method used to form a structure that does not have a counterdoped gate. Applicants respectfully submit that claim 34 is allowable over the teachings of Adkisson et al. and Fried et al. and request the withdrawal of the stated rejection.

Dependent claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. and Fried et al. as applied to claims 1 and 11 and further in view of Forbes et al. (U.S. Patent 6,414,356). Forbes was cited for the proposition of annealing a gate region before forming a metal. While anneals are known to drive dopants into materials, this combination of references does not teach the recitals of claim 15 and the underlying base claim limitations, as amended herein. Applicants request the withdrawal of the stated rejection.

New claims 35 and 36 are herein presented and recite a novel method not taught or suggested by the combination of references used above by the Examiner. For example, none of the art made of record teach or suggest "removing regions of the semiconductor layer having a substantially horizontal exposed surface". None of the art made of record teach or suggest a method of "doping the first and second physically separated sidewall spacers with two angled implants of opposite conductivity type". None of the art made of record using angled implants, or in which angled implants could theoretically be applied to, would eliminate at least one counterdoped region with a horizontal surface.

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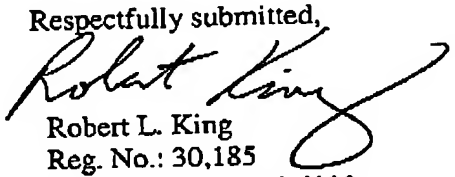
Applicants respectfully request consideration of the amendments and the allowance of claims 1, 2, 4, 5, 7-12, 14-21, 23-25 and 34-36, thereby placing the application in condition for allowance. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,



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